Rump Session: Advanced Silicon Technology Foundry Access Options for DoD Research

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Integration of IC Foundries and MEMS Fabrication

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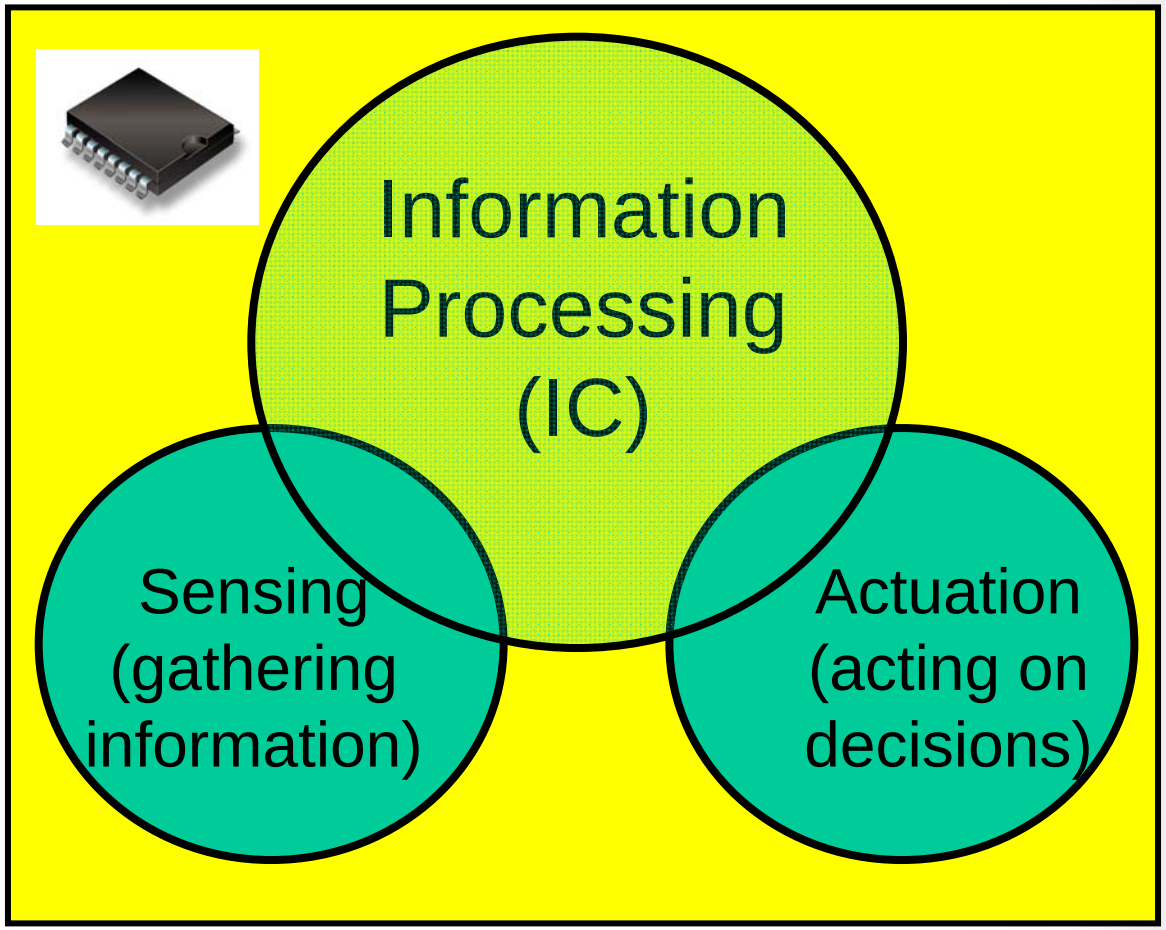
MTO Symposium 2009

RUMP Session: Advanced Silicon Technology Foundry Access Options for DoD Research

March 3, 2008
San Jose, California

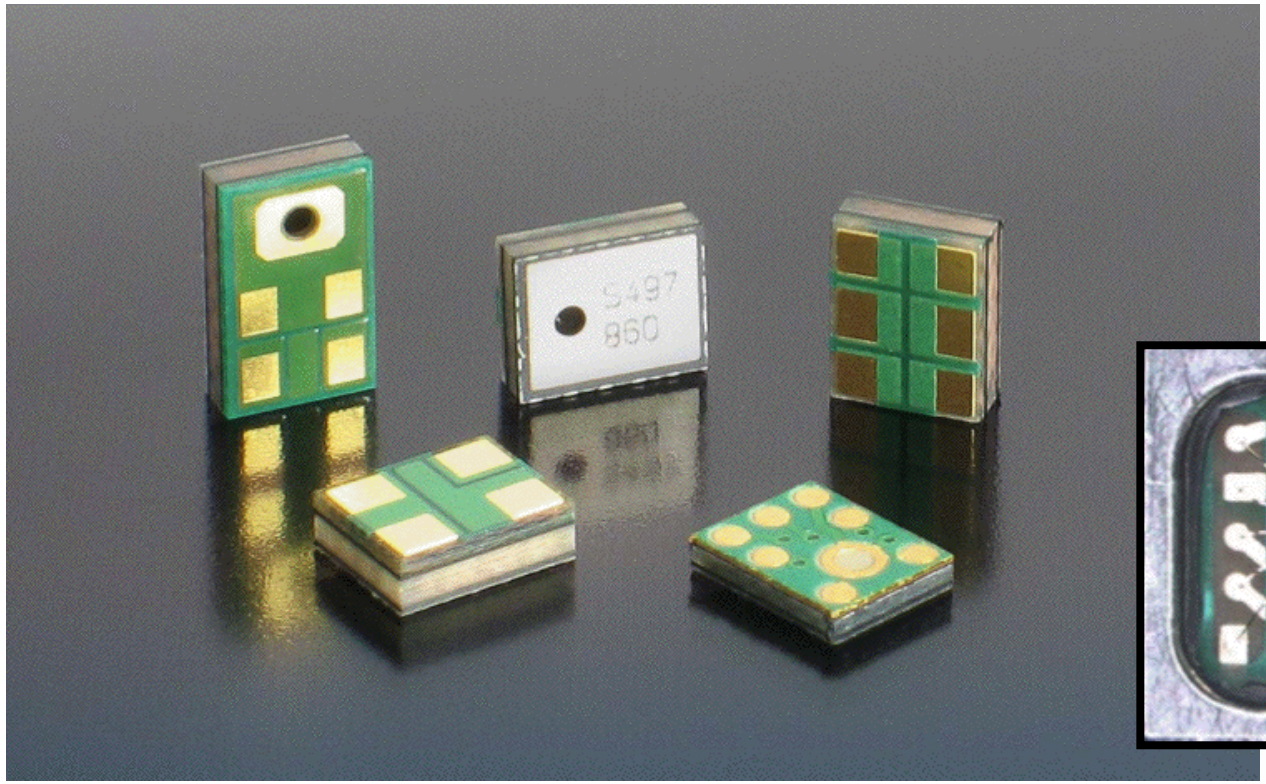
Microsystems Technologies

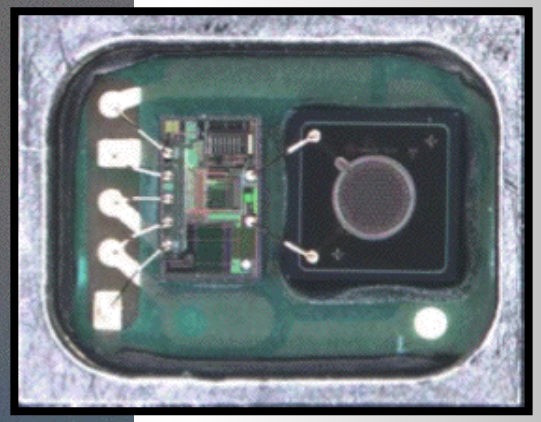


Fabrication of MEMS

- No Integration
  - Discrete Devices
- Co-Integration
  - System in a Package
- Monolithic Integration
  - System on a Chip

Example: Co-Integration

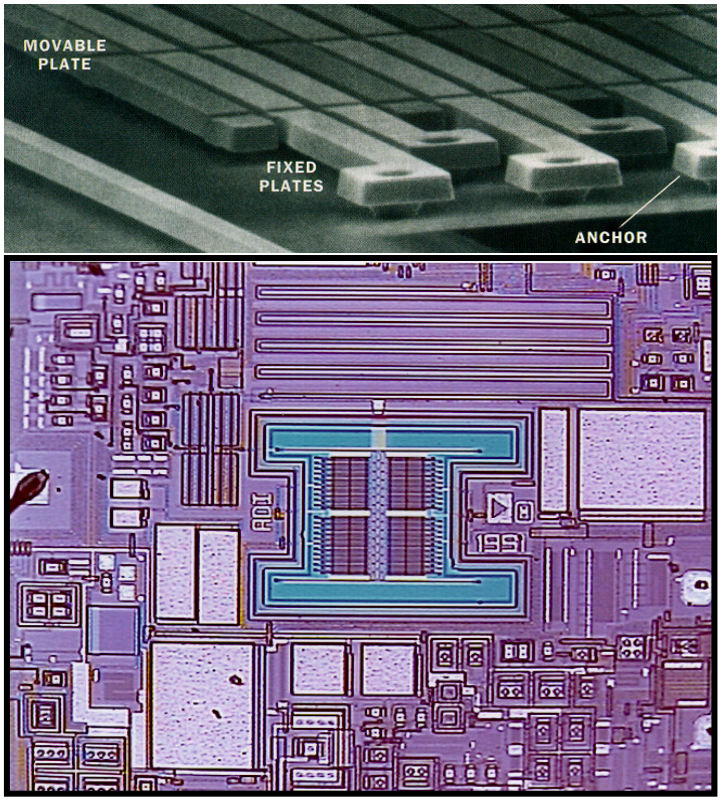




Dan Giesecke
Presentation to SEMI on MEMS Microphone

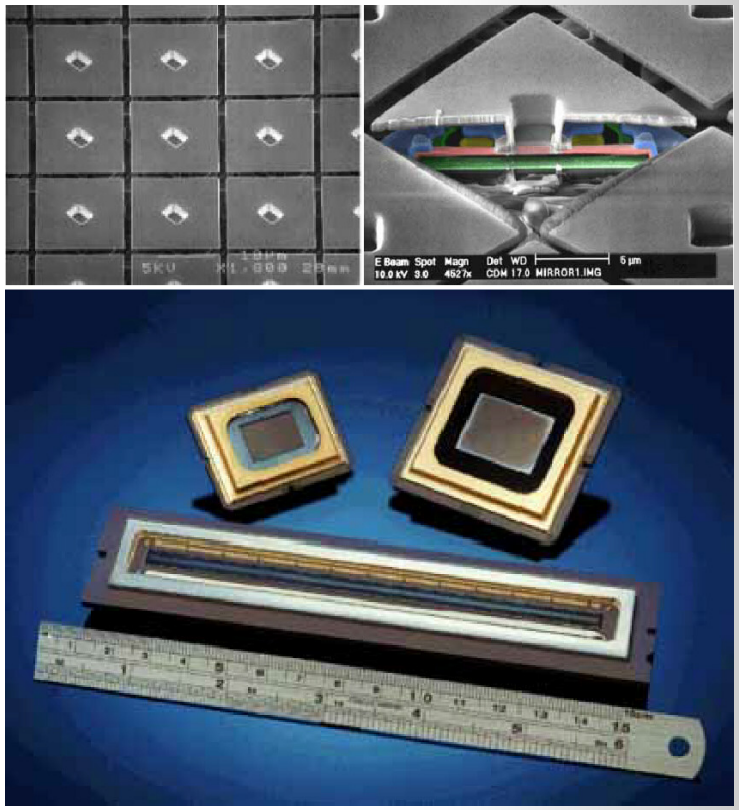
Knowles Acoustics
http://www.knowles.com/search/products/m_surface_mount.jsp

Example: Monolithic Integration



Analog Devices
Accelerometer

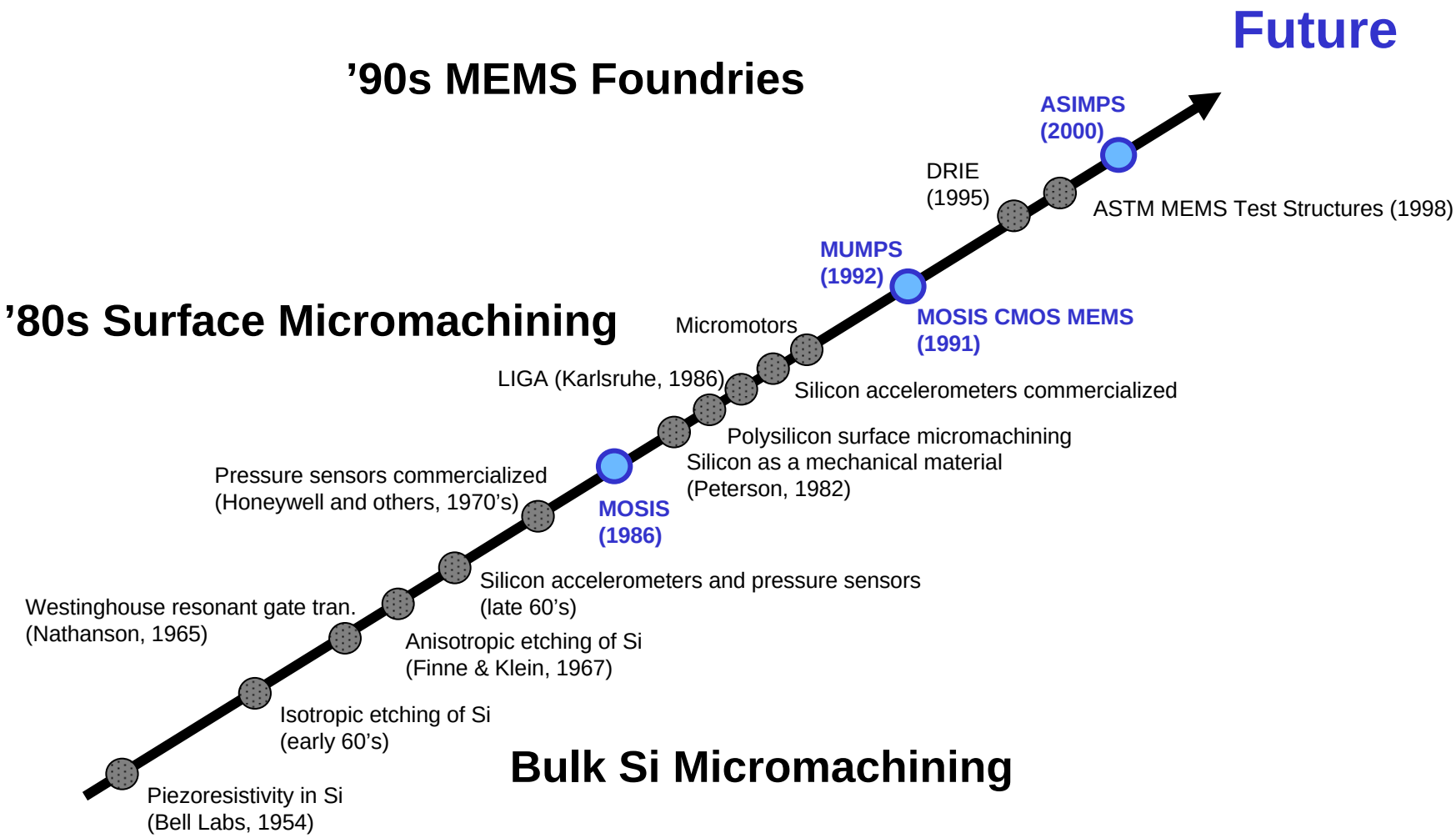
http://www.analog.com/mems



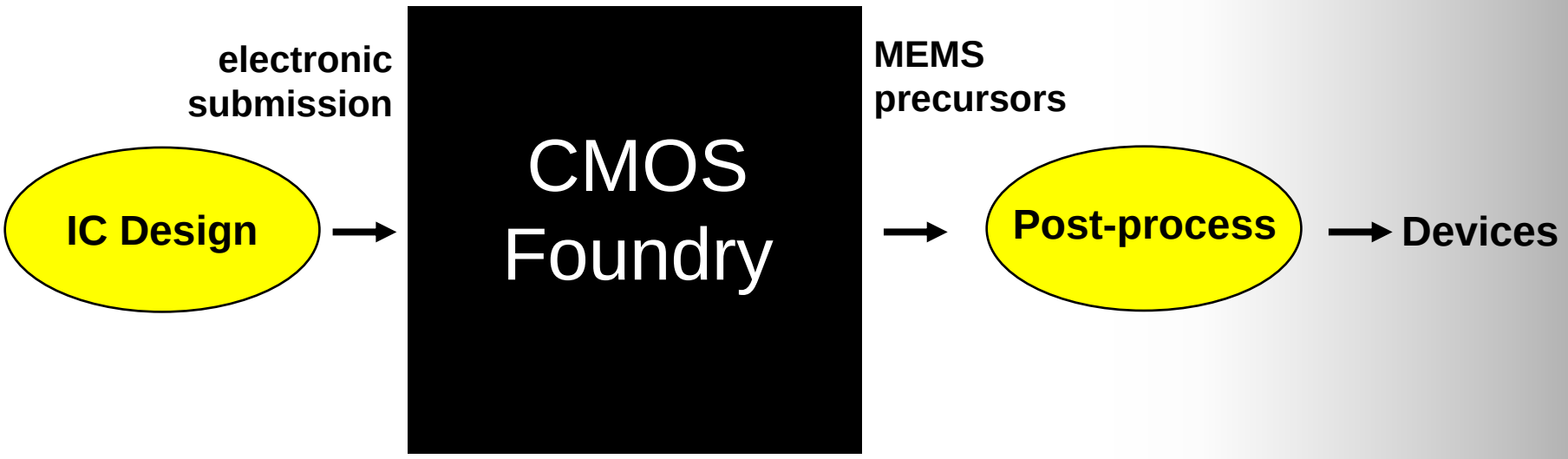
Texas Instruments
Deformable Mirror Display

http://www.dlp.com

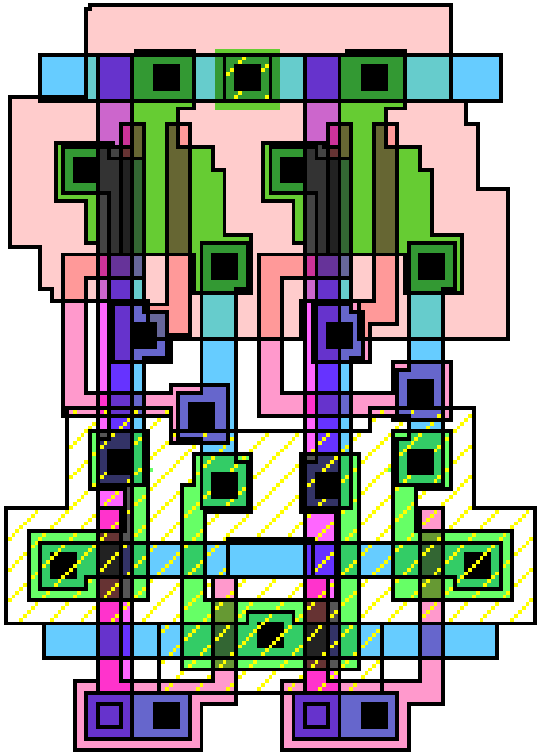
Timeline of Foundry Services

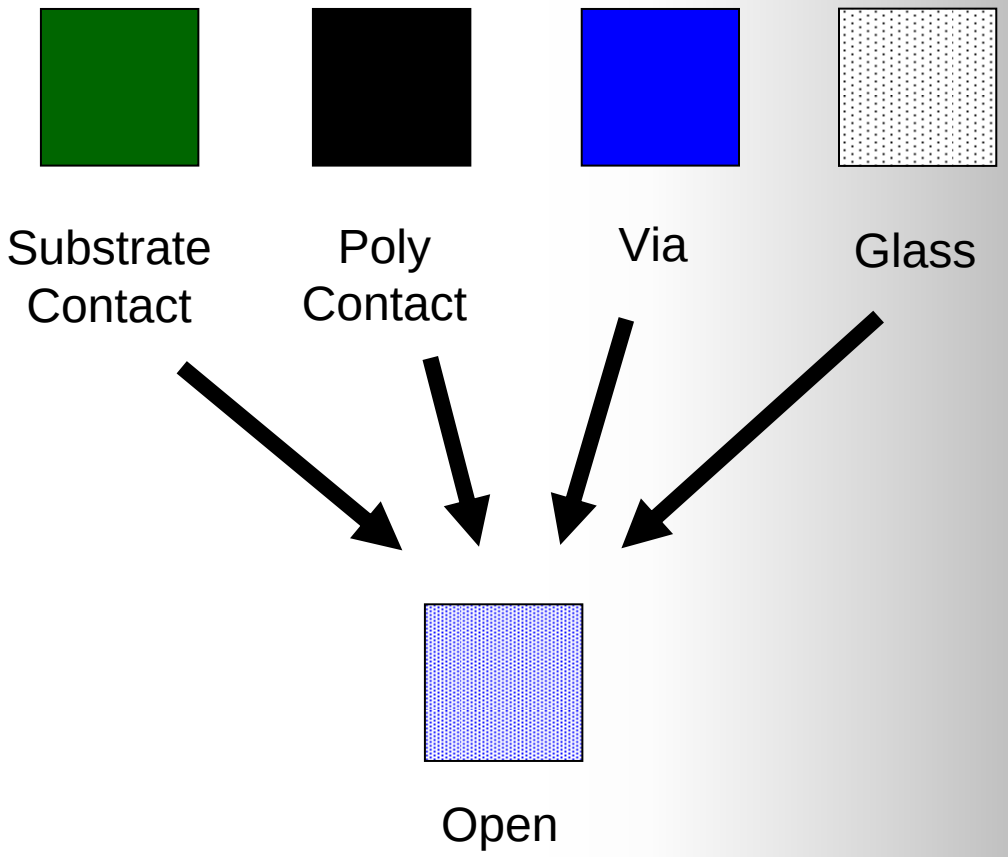


CMOS Foundry MEMS

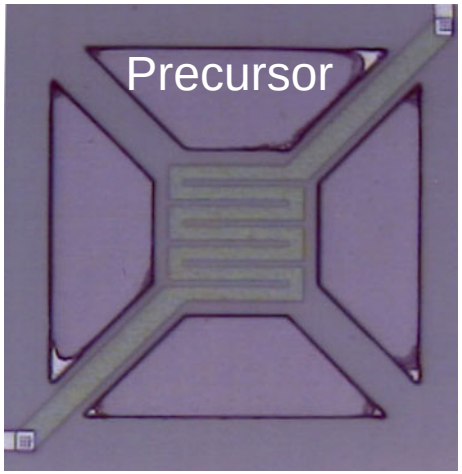


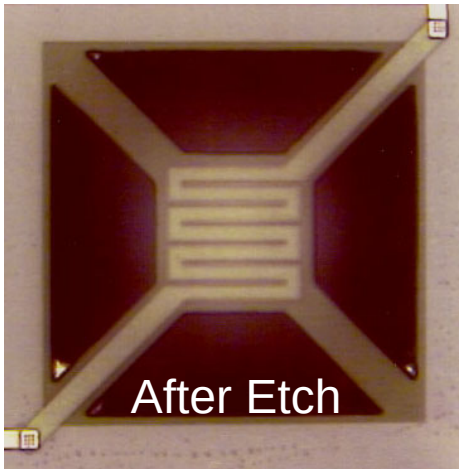
Design: Open Tile
(Stacked Via Opening)

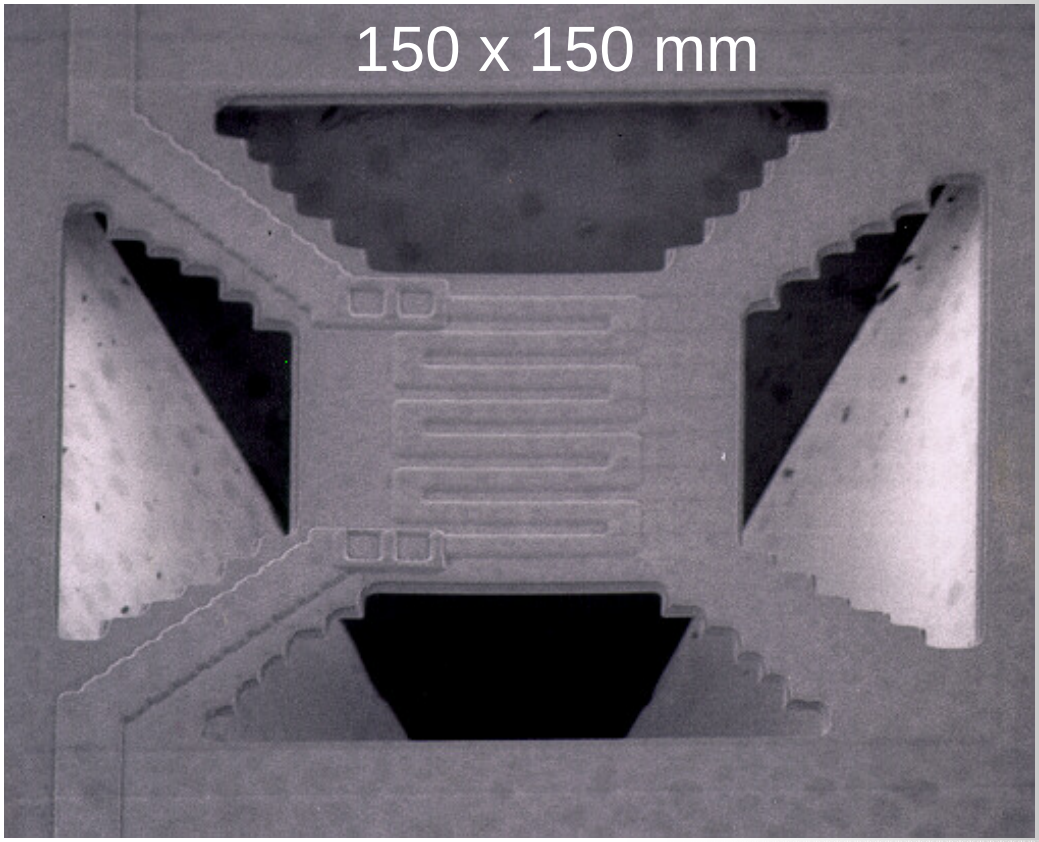




Example: Microheating Elements



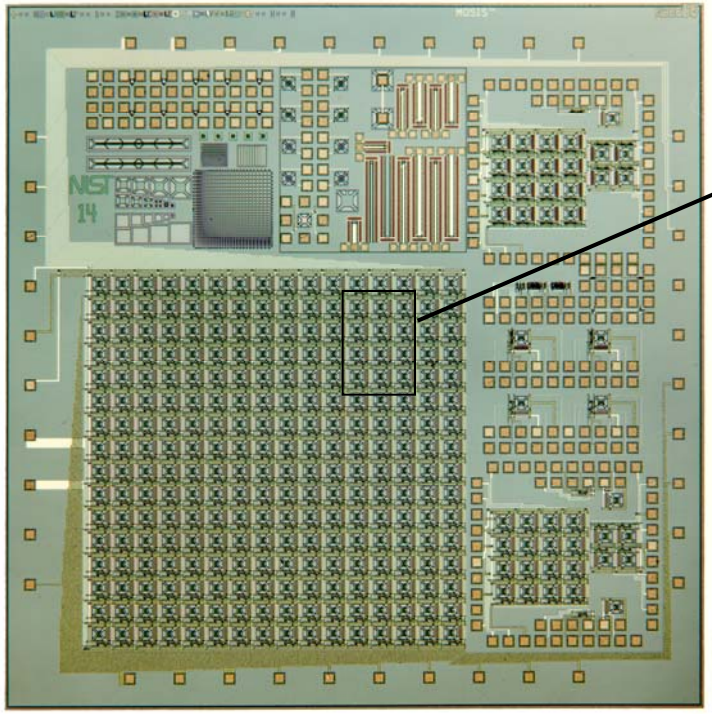


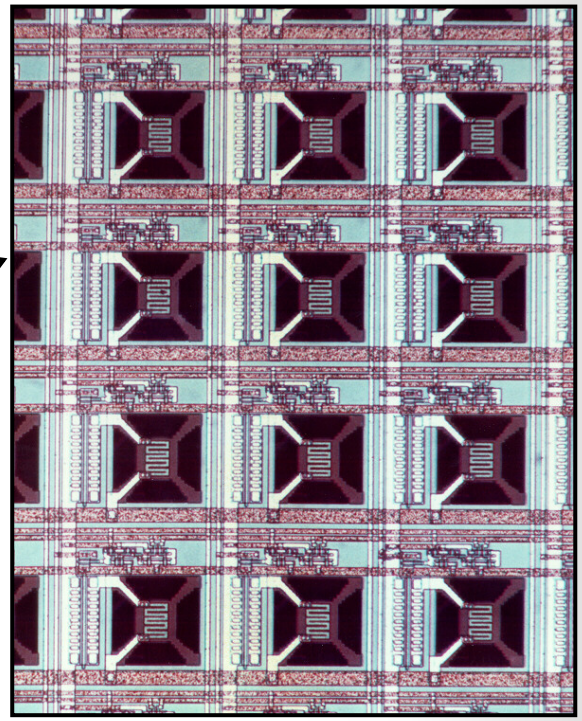


Parameswaren, Electron Device Letters, 12 (2), 57-59, Feb 1991.

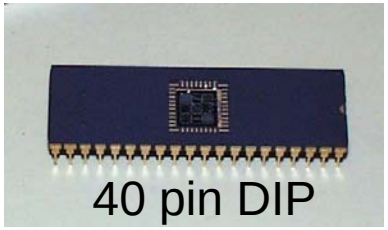
Thermal Array

16x16 Array





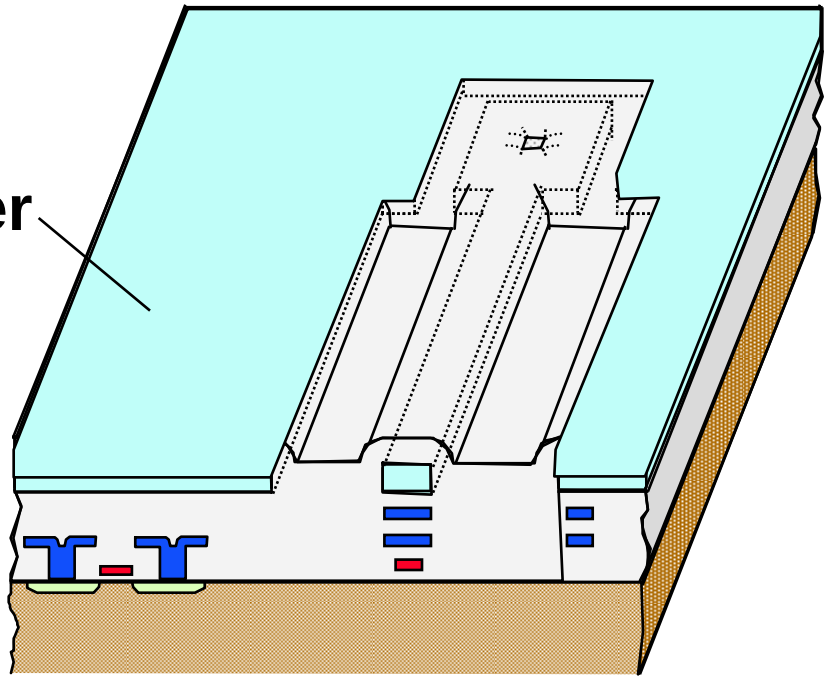
6x6 mm



ASIMPS Post-CMOS Micromachining

Application-Specific Integrated MEMS Process Service

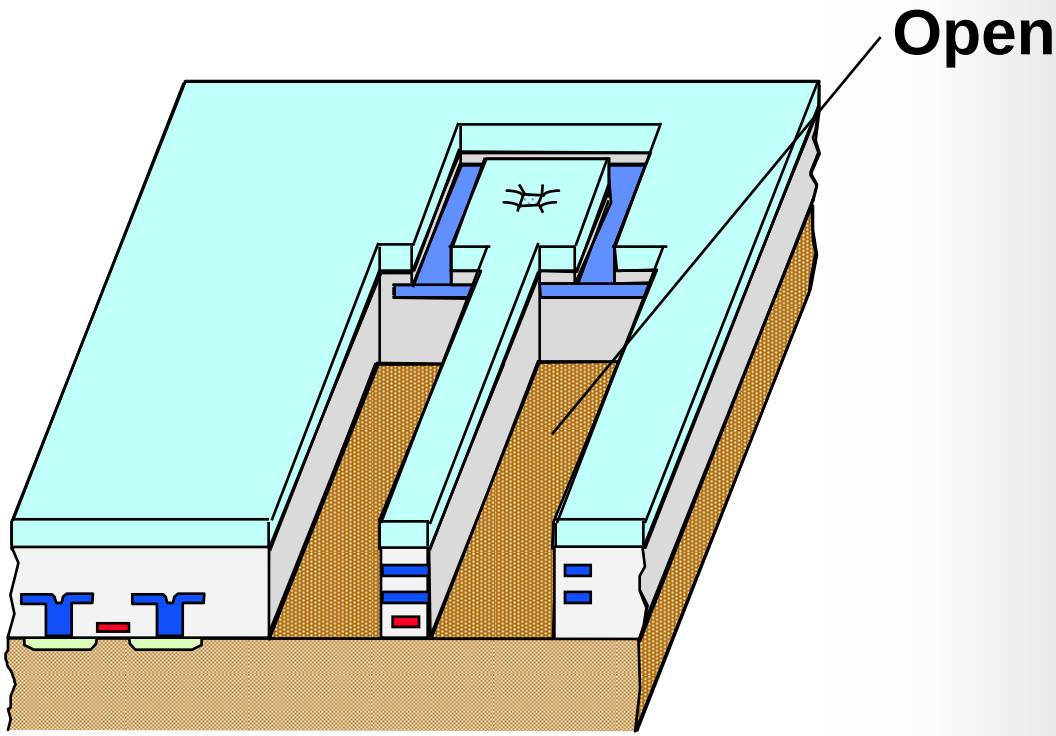
Metal mask layer



Carnegie Mellon University (CMU)

Fedder *et al.*, Sensors & Actuators A, v.57, no.2, 1996

ASIMPS Post-CMOS Micromachining

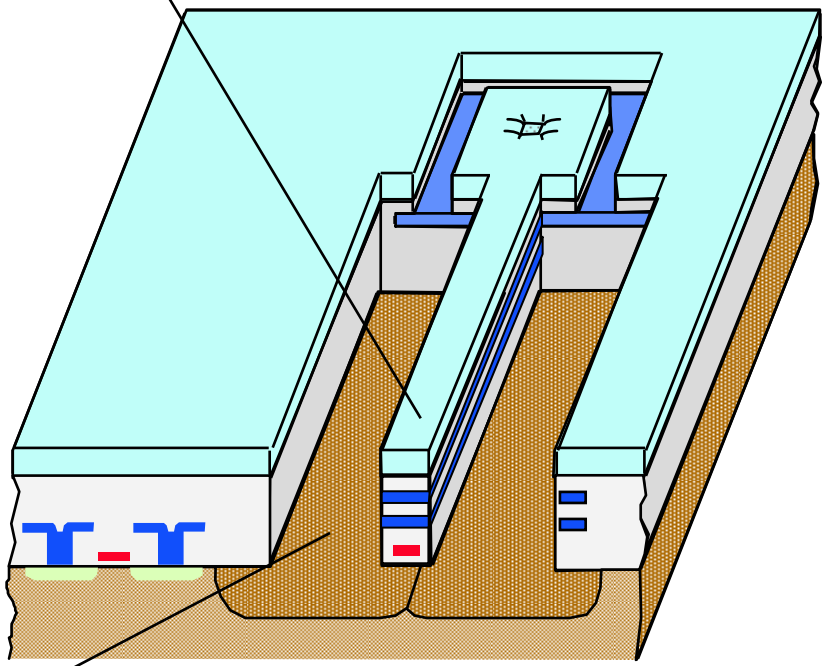


Carnegie Mellon University (CMU)

Fedder *et al.*, Sensors & Actuators A, v.57, no.2, 1996

ASIMPS Post-CMOS Micromachining

Composite beam

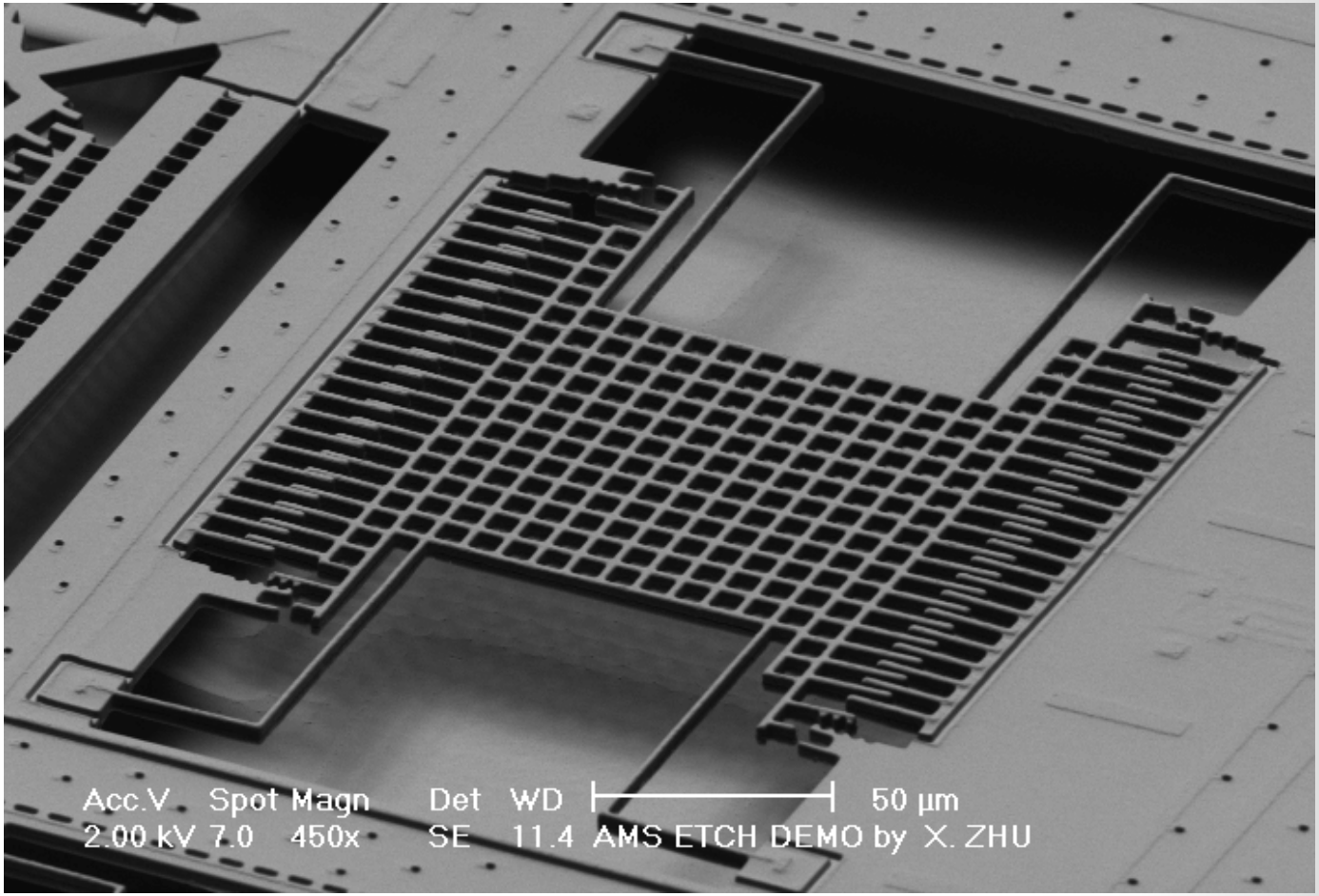


Anisotropically Etched

Carnegie Mellon University (CMU)

Fedder *et al.*, Sensors & Actuators A, v.57, no.2, 1996

ASIMPS Post-CMOS Micromachining

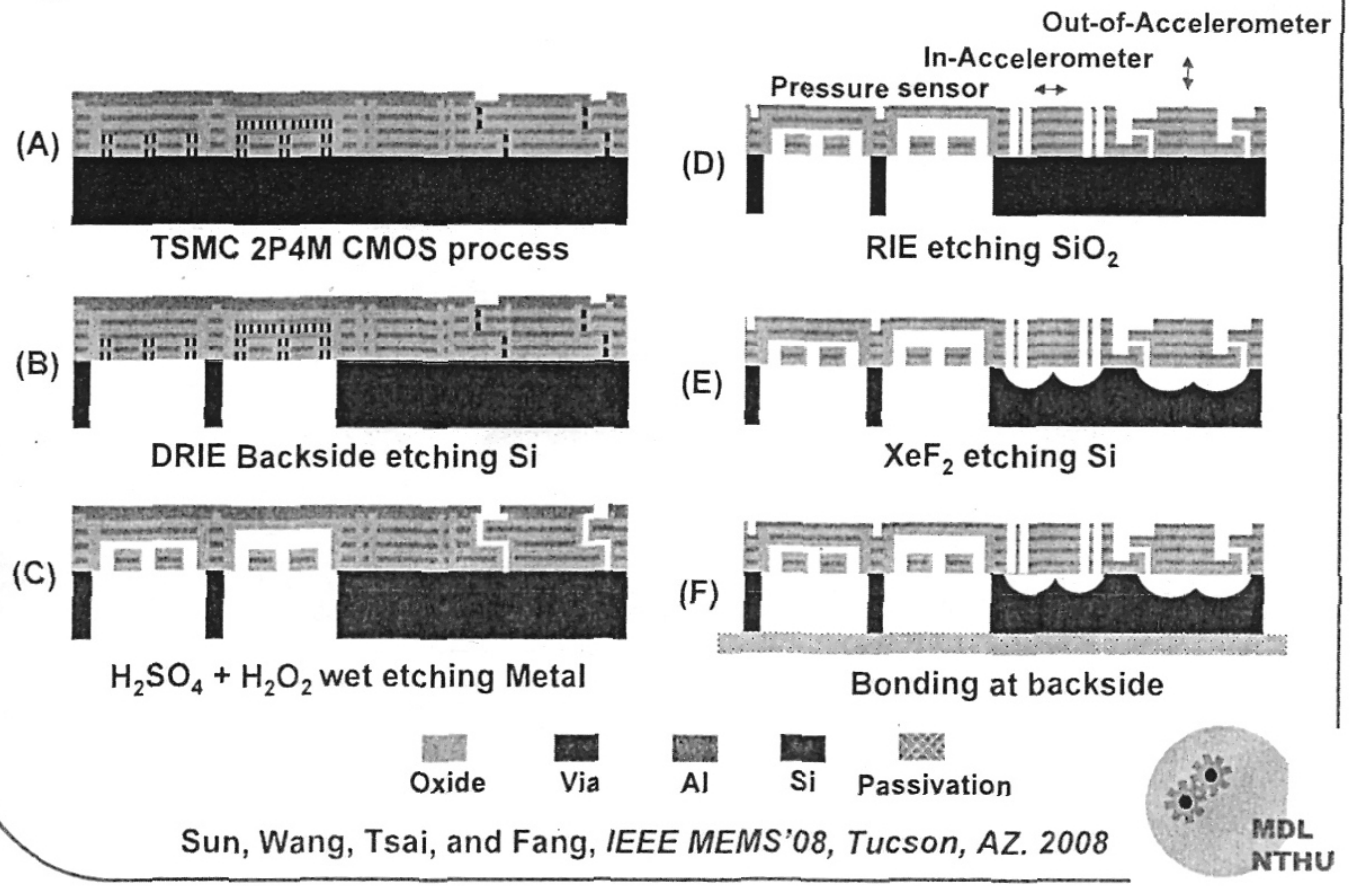


ASIMPS: AMS 0.6 mm, 3-metal

http://www.ece.cmu.edu/~mems/projects/asimps

TSMC CMOS MEMS

Double-side CMOS post processing



Sun, Wang, Tsai, and Fang, *IEEE MEMS'08, Tucson, AZ. 2008*

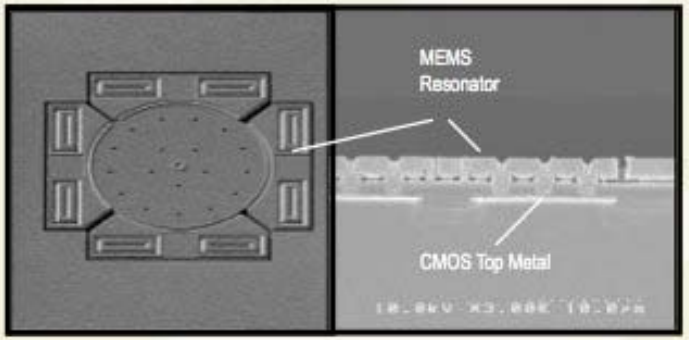
MDL NTHU

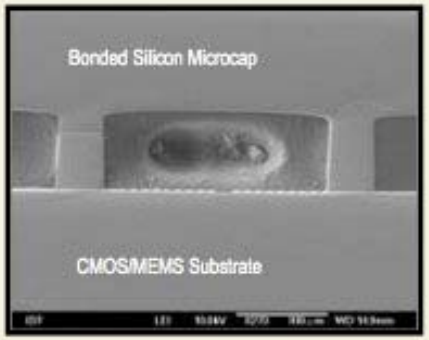
CMEMS™

SiGe deposited on top of CMOS

CMOS wafers + MEMS on top

Fabricate CMOS Wafer ⇨ **Back End of Line Integrated MEMS** ⇨ **MEMS Release and Eutectic Bonding Encapsulation**





- Wafers utilize existing, standard processes
- MEMS process independent of wafer technology

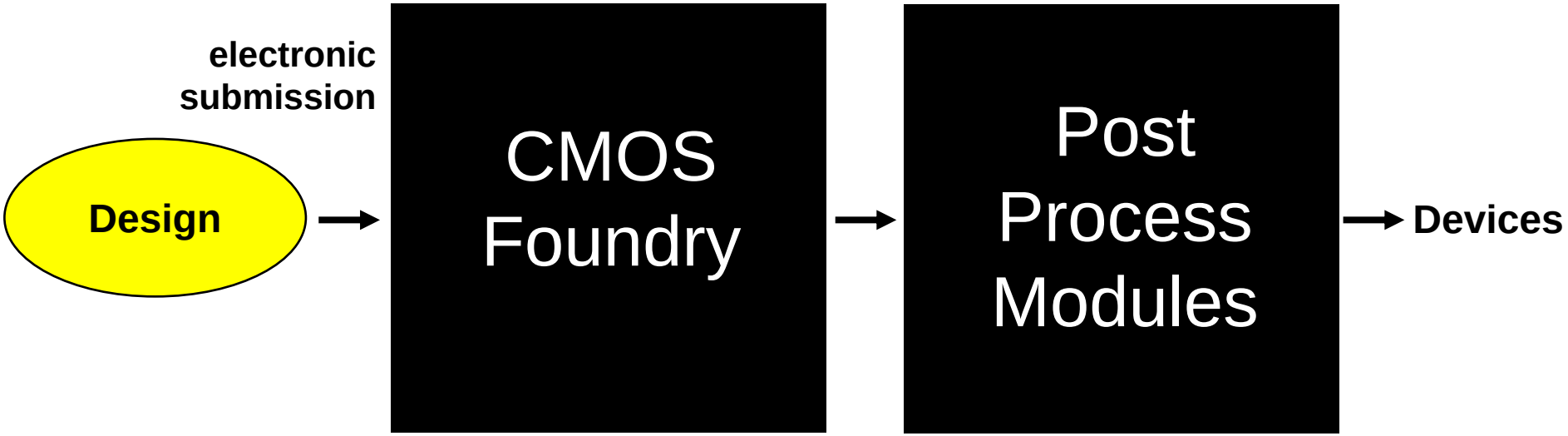
- Low temperature SiGe film deposition
- Modular, back-end compatible process
- Enables banks of multiple MEMS
- Integrate multiple MEMS functions (sensor, filter, etc.)

- Mainstream MEMS technique
- Compatible with standard plastic packaging
- Small form factor

SILICON CLOCKS

Emmanuel Quevy, Silicon Clocks

Moving Forward
Fully Supported Post Process Modules



Needed
- Affordability
- A variety of process flows
- Long term commitment
- CAD toolsets and design libraries
- Packaging

Summary

- CMOS MEMS post processes enable
  - Accessibility to monolithic integration
  - Device arrays with circuits
  - Circuits can be used to increase performance
- Issues
  - Co-Integrate or Integrate?
  - Can we live with (de facto) standard fabrication process modules?